

REMARKS

The indication that claims 29-44 contain allowable subject matter is greatly appreciated; however, for reasons to follow these claims have not been rewritten in independent form since it is believed that independent claim 20 is allowable over Ishihara et al.

The Examiner rejected claims 20-27 under 35 U.S.C. 102(b) as being anticipated by Ishihara et al. And, the Examiner rejected claim 28 under 35 U.S.C. 103(a) as being unpatentable over Ishihara et al. These rejections are respectfully traversed for the following reasons.

Claim 20 recites a method for determining a printing state of material on a substrate, comprising

printing material onto a required portion of a substrate and a test portion of said substrate ... **wherein said test portion corresponds to an area of said substrate that is at high risk of resulting in a defect of said material when printed thereon ... and wherein said material is printed onto said test portion under a condition that has a high risk of resulting in a defect of said material when printed on said test portion ...** and judging a printing state of said material printed onto said required portion by inspecting a printing state of said material printed onto said test portion. (emphasis added)

Such a method is not taught or suggested by Ishihara et al.

In this regard, Ishihara et al. discloses a method for detecting deterioration of solder paste printing. Specifically, on a printed circuit board PC a check pattern region 12 is defined in an area that is separated from a circuit pattern 5 that is on the printed circuit board. The check pattern region 12 can be either on a peripheral portion of the printed circuit board, or can be provided inside of the circuit pattern, so long as the check pattern region is separated from the circuit pattern 5. Solder paste 9 is printed onto the check

pattern region 12 through a mask 7 to provide a check pattern 21, and then this check pattern is monitored by inspection apparatus 2 for defects.

However, Ishihara et al. does not disclose or suggest that the check pattern region corresponds to an area that is at "high risk" of resulting in a defect of the solder paste when printed thereon. Indeed, because Ishihara et al. teaches that the check pattern region can be provided on any portion of the printed circuit board so long as the check pattern region is separated from the circuit pattern, Ishihara et al. is not concerned with providing the check pattern on a portion of the circuit board that is at high risk with regard to printing of solder paste thereon. Accordingly, for this reason alone claim 20 is not anticipated by Ishihara et al.

Additionally, Ishihara et al. does not disclose or suggest that the solder paste is printed onto the check pattern region under a condition that has a "high risk" of resulting in a defect of the solder paste. In this regard, the solder paste is printed onto the check pattern region by using a mask, and there is no discussion with regard to conditions under which the solder paste is applied to the check pattern region. Accordingly, Ishihara et al. is not concerned with printing solder paste onto the test pattern region under a condition that has a high risk with regard to printing of the solder paste. Thus, for this additional reason claim 20 is not anticipated by Ishihara et al.

Thus, it is respectfully submitted that claims 20-28 are allowable over Ishihara et al.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in condition for allowance and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicants' undersigned representative by telephone to resolve such issues.

Respectfully submitted,

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June 25, 2003